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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	Mills 11
First Inventor or Application Identifier	Allen P. Mills
Title	Method and Apparatus for Temperature Compensation of Read-Only Memory
Express Mail Label No.	EE 070 072 392US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 11] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]
4. Oath or Declaration [Total Pages]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* *[Note Box 5 below]*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(If applicable, all necessary)*
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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    [ ] Continuation [ ] Divisional [X] Continuation-in-part (CIP) of prior application No: 09/095,231
    Prior application information: Examiner _____ Group / Art Unit: _____

18. CORRESPONDENCE ADDRESS

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In re patent application of **MILLS**	: Atty Dkt: **MILLS 11**
Serial No.: **TBA**	: Date: **January 7, 2000**
Filed: **Herewith**	
For: **METHOD AND APPARATUS FOR TEMPERATURE COMPENSATION OF READ-ONLY MEMORY**	

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Rosangela Medina

METHOD AND APPARATUS FOR TEMPERATURE COMPENSATION OF READ-ONLY MEMORY

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. patent application, Serial No. 09/095231 entitled "RESISTIVE ELEMENT FOR SEMICONDUCTOR DEVICES," filed on June 10, 1998, and related to U.S. patent application, Serial No. 08/748,035 entitled "STRUCTURE FOR READ ONLY MEMORY," filed on November 12, 1996, which subsequently issued as U.S. Patent No. 5,847,442, which are assigned to the same assignee and are incorporated by reference herein.

FIELD OF THE INVENTION

This invention relates generally to electronic circuits and, more particularly, to temperature compensation of read-only-memory (ROM) electronic circuits.

BACKGROUND OF THE INVENTION

Read-Only Memories (ROMs) are well known in the art. Typically, ROMs are used in computer systems to provide a permanent storage of program instructions, such as mathematical functions, or informational data that is processed by mathematical functions. As is known in the art, a ROM typically consists of a planar array of parallel word lines, which are perpendicular to and insulated from a planar array of parallel bit

lines. In one embodiment of a ROM device, the two planes containing the word lines and bit lines are vertically disposed from each other and separated by an insulating layer. Active semiconductor devices such as bi-polar transistors or metal oxide semiconductor field effect transistors (MOSFETs) interconnect the junction of each word line and each bit line to form a memory cell. Typically, in the fabrication process, and for economy of scale, all the cells are populated with devices, and then a link to a particular device is opened in the encoding process to render that cell inactive. The connection or lack of connection of a device at a memory cell determines whether a logic "1" or "0" is stored in the cell. The control electrode (base or gate) of the active device is connected to the word line, and the emitter or source electrode is typically connected to the bit line, for transistor or MOSFET devices, respectively. A positive potential on a word line turns "on" the device at that cell. Where there is no physical link at the cell there is no signal transmitted to the bit line. The bit lines are then read in parallel to obtain a group of "1" and "0" signals that form the output of the ROM.

ROM devices may also be fabricated with resistive interconnections. U.S. Patent 5,847,442 to Mills, *et al.*, entitled "Structure for Read-Only Memories," which is incorporated by reference herein teaches a ROM device fabricated using resistive devices to interconnect word and bit lines. The use of resistive devices is advantageous over transistor devices as resistive devices are easier to fabricate and smaller in size. A brief summary of the incorporated reference is presented to provide a better understanding of the invention claimed herein.

A ROM device fabricated with resistive devices is illustrated in Figure 1 of the referred to U.S. Patent and is repeated herein as Figure 1. In the device shown, only

certain word lines **28** are connected to bit lines **40** by resistive device **30**. The connection between word line **28** and bit line **40** is specified by the specific data stored in the ROM device. Resistive device **30** is formed as a column, or post, within the insulating material that separates parallel word line **28** from the vertically disposed parallel bit line **40**.

Resistive device **30** may be fabricated within a wide range of values. In order to reduce cross-talk between word line **28** and bit line **40** the minimum value of resistance is in the order of tens of Megaohms. To achieve resistive values in the order of tens of Megaohms in the space allocated, resistive device **30** is typically comprised of a polysilicon material having a controlled resistivity. Polysilicon materials are well known in the art and, as is known, may be formulated in a doped or undoped condition. Doping elements are typically selected from a group of elements consisting of boron, phosphorous, arsenic, and antimony. As discussed in the referenced patent, a significant advantage of using a polysilicon post as a resistor device to interconnect word and bits lines is a decrease in the size of a memory cell as resistive devices are smaller and required less power than transistors or MOSFETs.

However, polysilicon is highly temperature sensitive, and, as is known in the art, the resistance of polysilicon decreases significantly with an increase in temperature. As the temperature increases and the resistivity of the connecting polysilicon resistive device decreases, the current through the resistive device increases. The increased current is known in the art to adversely affect the output voltage of the ROM as the output voltage is directly related to the current. One method of compensating for the increased output voltage is also disclosed in the aforementioned U.S. Patent. This method discloses using an operational amplifier with a gain characteristic responsive to the change in temperature

as sense amplifier **42**. As disclosed, the operational amplifier employs a feedback resistor with electrical and thermal characteristics similar to those of data resistor **30.** In this method, the gain of the operational amplifier decreases as the resistance of the feedback resistor decreases. The decreased gain compensates for the increased data current and maintains the output voltage substantially constant.

However, a disadvantage of this method of compensation is that the current flowing through the ROM device remains strongly related to the change in temperature. This change in current flow further affects the switching speed of the ROM device, and accordingly, the switching speed remains strongly influenced by the change in temperature.

SUMMARY OF THE INVENTION

The present invention relates to temperature compensation of Read-Only Memory (ROM) that uses a temperature sensitive resistive material to connect word and bit lines. In such devices, the change in temperature adversely affects the output voltage and the switching speed of the ROM.

In accordance with the invention, the current through a data resistive device is maintained at a substantially constant level by supplying to the ROM an input reference voltage that is responsive to changes in temperature. In one embodiment of the invention, an input reference voltage is developed by supplying a constant current source across a temperature-dependent reference resistor. The resistance of a reference resistor changes in response to changes in temperature and the voltage across the reference resistor (and

input to the ROM) changes accordingly. By changing the input voltage in response to a change in temperature, the data current to the ROM data resistors remains substantially constant. With a substantially constant current flow through the ROM device, the output voltage and ROM switching speed are maintained substantially constant.

In an exemplary embodiment of the invention, the reference resistor is made from a material that has a similar temperature-dependent resistivity as the material selected as the resistive device that interconnects word and bit lines within the ROM. In this embodiment of the invention, a change in resistance of the reference resistor matches a change in resistance of the data resistor, thus causing the current flow through the data resistor to remain substantially constant for any change in temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages, nature and various additional features of the invention will appear more fully upon consideration of the illustrative embodiments to be described in detail in connection with the accompanying drawings. In the drawings:

Figure 1 is a plan view of a ROM device constructed using resistive devices;

Figure 2 is a circuit diagram of one embodiment of the invention;

Figure 3 is a plan view of one embodiment of the invention illustrated in Figure 2 incorporated into the ROM device illustrated in Figure 1; and

Figure 4 is a second embodiment of the invention illustrated in Figure 2 incorporated in the ROM device illustrated in Figure 1.

It is to be understood that these drawings are for purposes of illustrating the inventive concepts of the present invention. It will be appreciated that the same reference numerals, possibly supplemented with reference characters where appropriate, have been used throughout the figures to identify corresponding parts.

DETAILED DESCRIPTION

Figures 1 through 4 and the accompanying detailed description contained herein are to be used as illustrative examples of exemplary embodiments of the present invention and should not be construed as the only manner of practicing the invention.

Referring now to Figure 2, there is shown an exemplary embodiment of the invention. In this embodiment of the invention, switch **25** is used to translate a command on an input address line **24** to a voltage on word line **28**. In the exemplary embodiment of the invention illustrated, a MOSFET switch is used to translate an address line command to a word line voltage. As would be understood by those skilled in the art, a plurality of different switch types, using different technologies, may be used to translate an address line command to a word line voltage. For example, CMOS, Bi-polar transistor, diodes, mechanical and electro-static switches may be used in accordance with the invention. In this illustrated embodiment, when switch **25** is gated high (*i.e.*, on) the current I_a, generated by constant current source **27,** flows through the switch to ground. However, when the illustrated switch is gated low (*i.e.*, off) then current, I_a, develops a reference voltage, V_r, across reference resistor **29** that is applied as input voltage, V_i, to

driver **26**. As illustrated, driver **26** is represented as an unity gain operational amplifier configured as a voltage follower. As is known in the art, the voltage V_i at the high impedance input of the amplifier is present at the low impedance output of the amplifier. Hence, the reference voltage is present at the input side of data resistor **30**.

In accordance with one embodiment of the invention, reference resistor **29** is a temperature-dependent resistor having similar properties of conductivity as data resistor **30**. As the temperature changes, the resistive value of reference resistor **29** changes and the voltage developed across reference resistor changes in direct relation to the change in resistance. In the specific case that data resistor **30** and reference resistor **29** have the same electrical and thermal characteristics, upon gating switch **25** off the driver voltage V_r appears on word line 25 and current I_a flows from an input line (word line **28**) to an output line (bit line **40**) through data resistor **30.** Current I_a is then supplied to sense amplifier **42** to produce an output voltage. Sense amplifier **42**, in this exemplary illustration of the present invention, is an operational amplifier with a fixed, temperature-independent, resistor **41**. As is known in the art, the output voltage of sense amplifier **42** may be determined from the value of the fixed feedback resistor **41** and the current I_a as:

$$V_{out} = -I_a R$$

where R is the value of feedback resistor **41**.

In accordance with one embodiment of the invention, reference resistor **29** is formed from a material with substantially similar properties of conductivity as those of data resistor **30**. In this case, the resistance values of data resistor **30** and reference resistor **29** change at substantially the same rate in response to a change in temperature. Accordingly, with constant current I_a supplied to reference resistor **29**, the voltage

developed across reference resistor **29** at any temperature is substantially the same as the voltage drop across data resistor **30** caused by current I_a flowing through data resistor **30.** The input reference voltage is thus adjusted at a rate that maintains current I_a substantially constant through data resistor **30** when the associated word line is selected.

Figure 3 illustrates one embodiment of the present invention incorporated in a resistive device ROM illustrated in Figure 1. In this embodiment of the invention, a temperature compensation circuit of the type illustrated in Figure 2 is connected to each input word line **28** through driver amplifier **26**. In this illustrated embodiment, inputs **20** provide commands to an n-stage ring counter **22** having a series of outputs connected to address lines **24**. Address lines **24** are then connected, in this illustrated embodiment to a series of MOSFET switches **25**, one switch for each address line. Coupled to each switch, is a reference resistor **29**.

As discussed previously in regard to Figure 2, reference voltage V_r is developed across reference resistor **29** by supplying a constant current to temperature-dependent reference resistor **29**, when the illustrated switch **25** is gated low. When switch **25** is gated high, the reference voltage is nominally at ground level. Reference voltage V_r is then used as input voltage V_i to driver **26**. Drivers **26** are typically in a low output state and each driver, when turned on, produces an output voltage V_0 that follows the input voltage, V_i. In accordance with one embodiment of the invention, V_i is either a nominally zero level when a selected MOSFET switch **25** is gated on or a nominally V_r level when a selected MOSFET switch **25** is gated off.

As discussed in the referenced U.S. Patent, word line **28** is insulated from the bit line **40** except at selected cell sites where a connection is made between a word line and a

bit line by data resistor **30**. At the memory cells where data resistor **30** is present, current I_a flows from word line **28** to bit line **40**. Current I_a is then conveyed sense amplifier **42** by bit line **40**.

In this illustrated embodiment of the invention, sense amplifier **42** is a feedback operational amplifier with a gain determined by feedback resistor **41**. As would be understood in the art, sense amplifier **42** may be operated either in a linear or non-linear mode. In the shown embodiment, feedback resistor **41** is a fixed value, and is substantially independent of temperature. The output voltage of sense amplifier **42** may then be determined from current I_a and feedback resistor **41**. As both the current I_a and resistor **41** are temperature-independent, the output voltage remains substantially constant.

Figure 4 illustrates a second embodiment of the invention as applied to a ROM device illustrated in Figure 1. In this embodiment of the invention, a single constant current source **27** and reference resistor **29** are used to generate reference voltage V_r. Reference voltage V_r is then applied to each word line **28** through, in this illustrated embodiment, CMOS switch **25**. As illustrated, CMOS switch **25** is implemented as an inverter composed of two complementary MOSFET switches **62** and **64**. In this embodiment, when a selected address line **24** is high, switch **64** is gated off and switch **62** is gated on. Accordingly, the voltage level at the input to drive **26** and, correspondingly, word line **28** is nominally at a ground level. However, when a selected address line **24** is low switch **64** is gated on and MOSFET switch **62** is gated off. In this case, the voltage level at the input to drive **26** and, correspondingly, on word line **28** is nominally reference voltage V_r. This embodiment of the invention is advantageous over that illustrated in

Figure 3 as the same reference voltage is selectively applied to each of the plurality of input drivers **26**.

In the specific case of a ROM employing polysilicon data resistors, it is further advantageous to operate the data resistor in a non-linear region. Properties of polysilicon are well known in the art. As is known in the art, the current through a polysilicon resistor is determined as:

$$I(v) = \hat{I}_o \sinh\left(\frac{V}{V_o}\right) \qquad [1]$$

$$\text{where } \hat{I}_o = a * exp\left(\frac{-E_0}{kT}\right); \qquad [2]$$

V_0 is proportional to the absolute temperature, T;

k is Boltzmann's constant; and

E_0 is approximately 0.5 eV, which is approximately half the bandgap of silicon.

From Equation 1 it would be understood by one skilled in the art that when the voltage, V, is greater than V_0, then the resistance in the polysilicon material is non-linear. A more detailed presentation of the properties of polysilicon materials may be found in Chapter 5 of "Polycrystalline Silicon for Integrated Circuit Applications," Ted Kamins, Kluwer Academic Publishers, Boston, 1988. Furthermore, it is understood from Equations 1 and 2, that the current, $I(v)$, is exponentially related to the voltage and the inverse of temperature, therefore, large changes in resistive value are compensated by small changes in voltage. In still another embodiment of the invention, the current flowing through data resistor **30** may be proportional to the input current I_a.

As would be understood by those skilled in the art, the reference voltage, V_r, may be generated by analog or digital means from locally measured temperature. Further still, the reference voltage may be developed externally or internally to the ROM. In a preferred embodiment of the invention, polysilicon reference resistors and an analog method are used to generate the reference voltage.

The examples given herein are presented to enable those skilled in the art to more clearly understand and practice the instant invention. The examples should not be considered as limitations upon the scope of the invention, but as merely being illustrative and representative of the use of the invention. Numerous modifications and alternative embodiments of the invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention and is not intended to illustrate all possible forms thereof. It is also understood that the words used are words of description, rather than limitation, and that details of the structure may be varied substantially without departing from the spirit of the invention and the exclusive use of all modifications which come within the scope of the appended claims is reserved.

WHAT IS CLAIMED IS:

1. In a ROM device using a plurality of data resistors to interconnect a plurality of input word lines with a plurality of output bit lines, a temperature compensation circuit to maintain a current through a selected one of said data resistors substantially constant comprising:

at least one reference resistor, wherein the conductivity of said reference resistors is responsive to changes in temperature;

a constant current source coupled to said at least one reference resistor, said constant current source developing a voltage across said at least one reference resistor; and

at least one switch connected to said at least one reference resistor to selectively couple said voltage to said input word lines.

2. A temperature compensation circuit as recited in Claim 1 wherein conductive properties of said reference resistor are selected to be the same as the conductive properties of said data resistors.

3. A temperature compensation circuit as recited in Claim 2 wherein said data resistor is selected from a polysilicon material.

4. A temperature compensation circuit as recited in Claim 3 wherein said polysilicon material is undoped.

5. A temperature compensation circuit as recited in Claim 3 wherein said polysilicon material is doped.

6. A temperature compensation circuit as recited in Claim 2 wherein said data resistor is comprised of a metal oxide.

7. A temperature compensation circuit as recited in Claim 1 wherein conductive properties of said reference resistor s are selected to be substantially similar to the conductive properties of said data resistors.

8. A temperature compensation circuit as recited in Claim 7 wherein said data resistor is selected from a polysilicon material.

9. A temperature compensation circuit as recited in Claim 8 wherein said polysilicon material is undoped.

10. A temperature compensation circuit as recited in Claim 8 wherein said polysilicon material is doped.

11. A temperature compensation circuit as recited in Claim 7 wherein said data resistor is comprised of a metal oxide.

12. A temperature compensation circuit as recited in Claim 1 further comprising:

a plurality of sense amplifiers coupled to said output bit lines, each output line having at least one sense amplifier, said sense amplifier receiving said constant current flowing through said data resistors wherein each of said sense amplifier provides a constant output voltage.

13. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier comprises

an operational amplifier with a fixed feedback resistor, R, wherein said amplifier output voltage is determined from the value of said constant current and said feedback resistor.

14. A temperature compensation circuit as recited in Claim 13 wherein said feedback resistor is temperature independent.

15. A temperature compensation circuit as recited in Claim 1 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is high.

16. A temperature compensation circuit as recited in Claim 1 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is low.

17. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier is operated in the non-linear region.

18. A temperature compensation circuit as recited in Claim 12 wherein said sense amplifier is operated in the linear region.

19. A method to maintain a current through Read-Only Memory (ROM) substantially constant as temperature changes wherein said ROM employs a plurality of data resistors to provide electrical interconnections between a plurality of input lines and output lines, comprising the steps of:

selecting a reference resistor having substantially similar properties of conductivity as said data resistor;

supplying a reference voltage to said input lines, said reference voltage developed by supplying a constant current to said reference resistor, wherein said reference voltage is responsive to a change in temperature.

20. The method as recited in Claim 19 wherein said data resistor is comprised of undoped polysilicon.

21. The method as recited in Claim 19 wherein said data resistor is comprised of doped polysilicon.

22. The method as recited in Claim 19 wherein the step of supplying said reference voltage further comprises the step of selectively switching said reference voltage to said word line.

23. In a ROM device using a plurality of data resistors to interconnect a plurality of input word lines with a plurality of output bit lines, a temperature compensation circuit to maintain a current through a selected one of said data resistors substantially constant comprising:

at least one voltage source producing a voltage that is responsive to changes in temperature; and

at least one switch connected to said at least one voltage source to selectively couple said voltage to said input word lines.

24. A temperature compensation circuit as recited in Claim 23 further comprising:

a plurality of sense amplifiers coupled to said output bit lines, each output line having at least one sense amplifier, said sense amplifier receiving said

constant current flowing through said data resistors wherein each of said sense amplifier provides a constant output voltage.

25. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier comprises

an operational amplifier with a fixed feedback resistor, R, wherein said amplifier output voltage is determined from the value of said constant current and said feedback resistor.

26. A temperature compensation circuit as recited in Claim 25 wherein said feedback resistor is temperature independent.

27. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier is operated in the non-linear region.

28. A temperature compensation circuit as recited in Claim 24 wherein said sense amplifier is operated in the linear region.

29. A temperature compensation circuit as recited in Claim 23 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is high.

30. A temperature compensation circuit as recited in Claim 23 wherein said at least one switch selectively couples said voltage to a selected one of said input word lines when an input to said switch is low.

31. A temperature compensation circuit as recited in claim 23 wherein said temperature responsive voltage changes to compensate for changes in voltage across said data resistor.

32. A method to maintain a current through Read-Only Memory (ROM) substantially constant as temperature changes wherein said ROM employs a plurality of data resistors to provide electrical interconnections between a plurality of input lines and output lines, comprising the steps of:

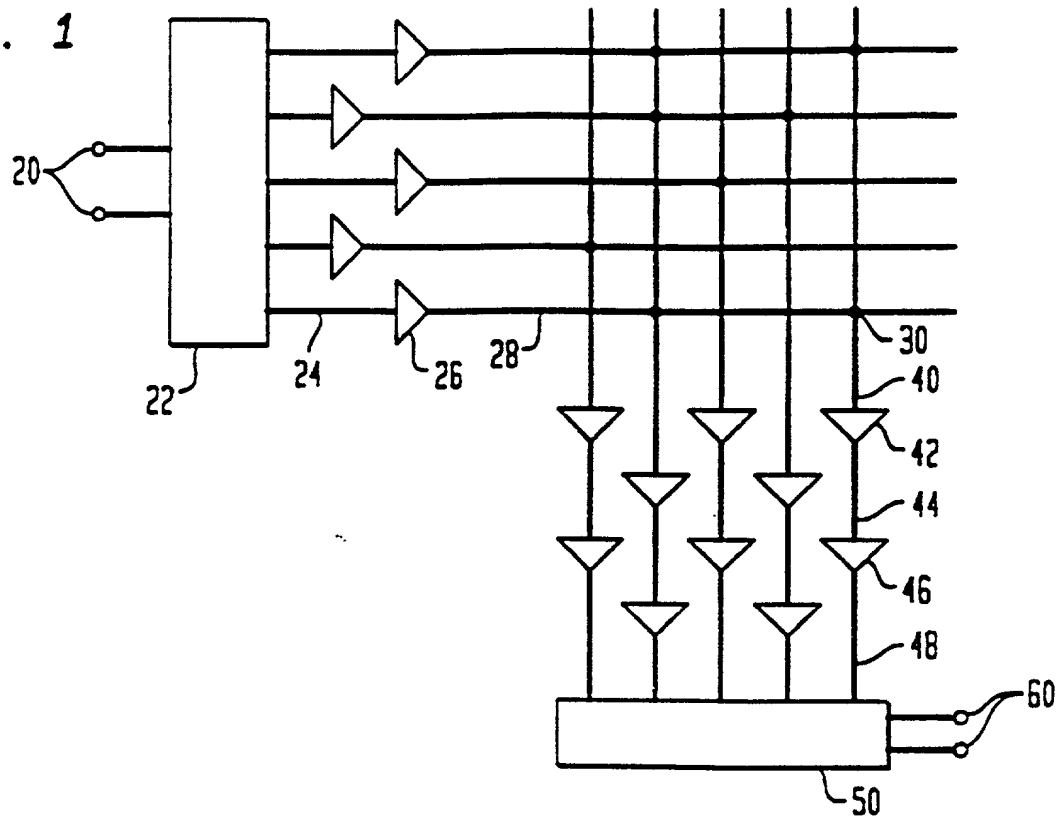
supplying a reference voltage that is responsive to changes in temperature to said input lines, wherein said reference voltage changes to maintain said current through said data resistor substantially constant.

33. The method as recited in Claim 32 wherein the step of supplying said reference voltage further comprises the step of selectively switching said reference voltage to said word line.

ABSTRACT

A method and apparatus for temperature compensation of a resistive based Read-Only Memory device is disclosed. In accordance with the method of the invention, the input voltage supplied to ROM device is adjusted in response to changes in temperature to maintain the current through the ROM at a substantially constant level even as the resistivity of the temperature-dependent connection resistors changes. In one embodiment of the invention, the voltage across the reference resistor is determined by providing a constant current source to the reference resistor and this voltage level is applied to the input of the ROM device. The reference resistor is selected to have similar properties of conductivity as those of the data resistor, for example, a polysilicon. As the temperature increases, the resistivity of a polysilicon data resistor and resistor decrease in a similar manner and, accordingly, the voltage across the reference resistor also decreases. The voltage across the reference resistor decreases at a rate commensurate with a decreased voltage drop across the data resistor, thus maintaining the current through a selected data resistor constant.

FIG. 1



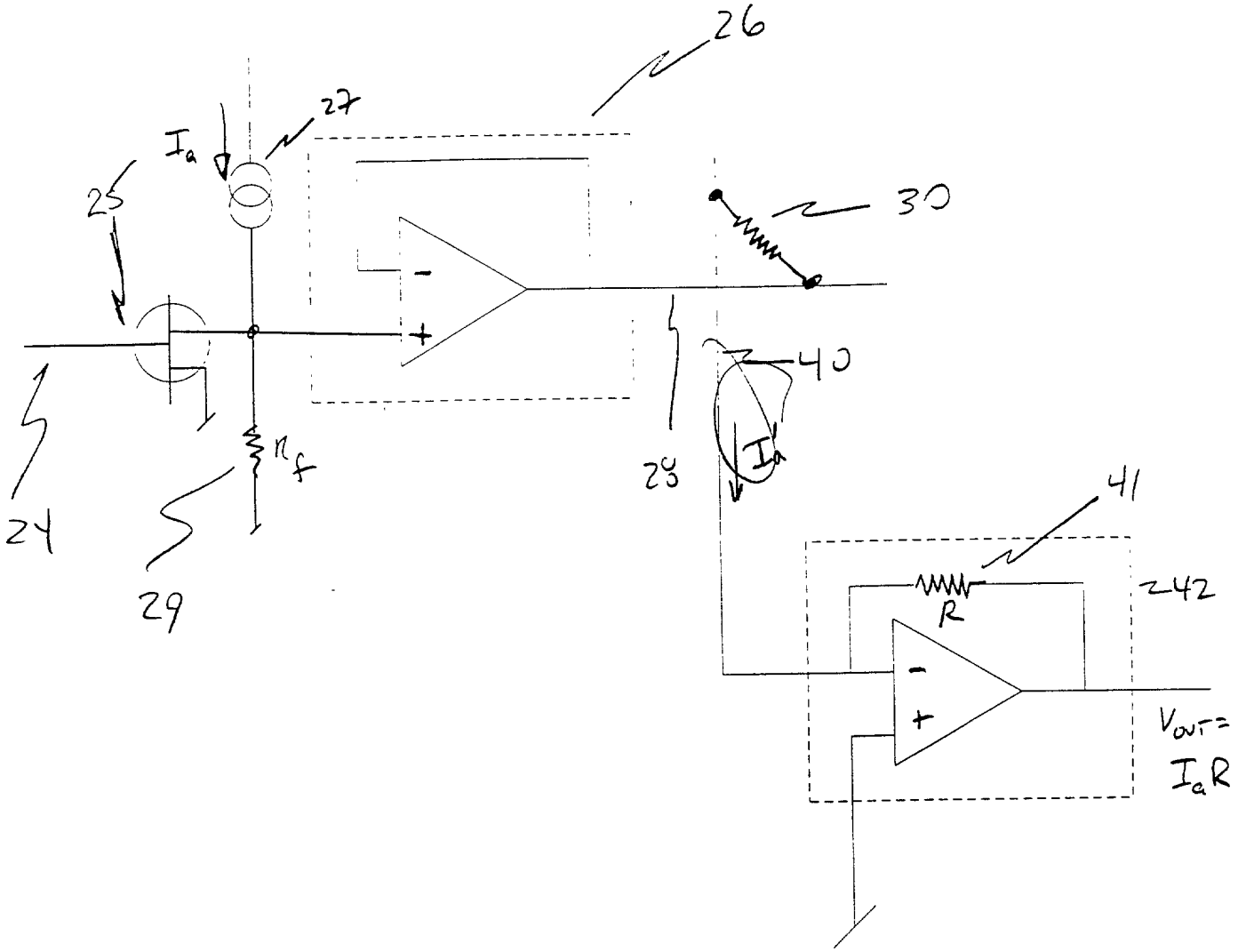


Figure 2

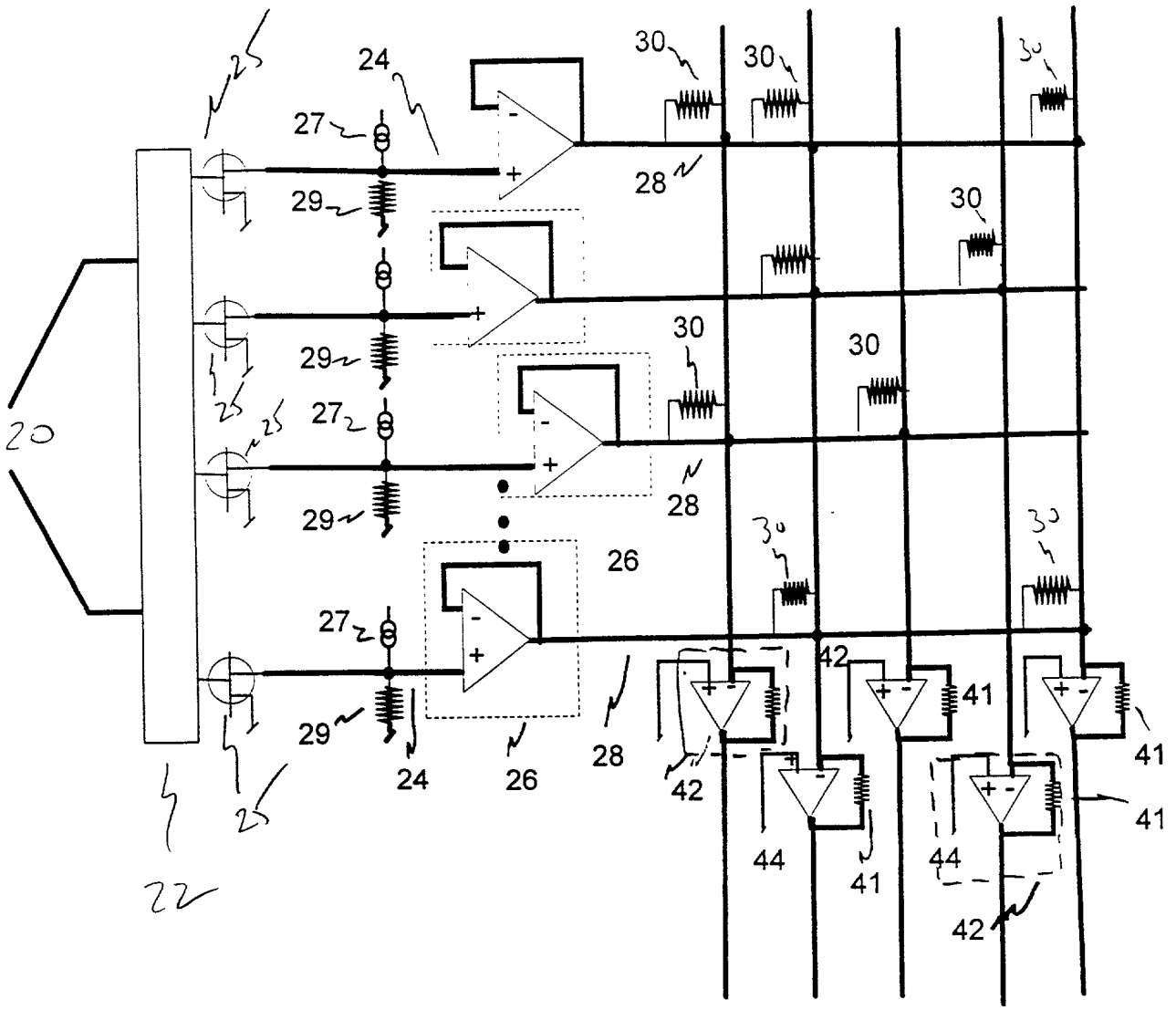


Figure 3

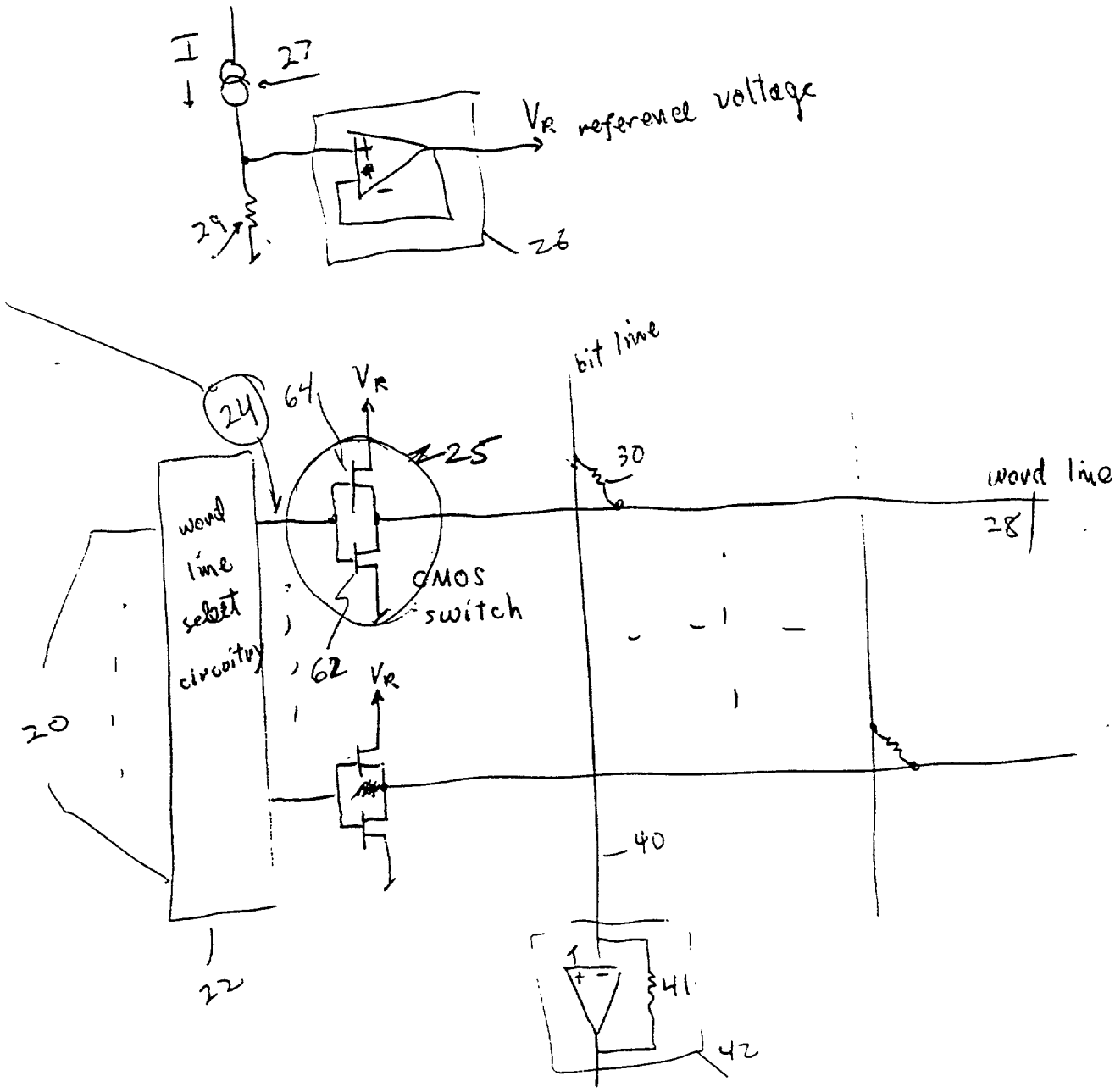

I
27
V_R reference voltage
29
26
24
64
V_R
25
bit line
30
word line
28
word line select circuitry
CMOS switch
62
V_R
20
40
22
41
42

Fig 4

IN THE UNITED STATES
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As the below named inventor, I hereby declare that:

My residence, post office address and citizenship is as stated below next to my name.

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

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None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby appoint the attorney(s) on ATTACHMENT A as associate attorney(s) in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorney(s) and such associate attorney(s) are specifically denied any power of substitution or revocation.

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Inventor's signature Allen P. Mills Jr Date Jan 4, 2000

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